

SC Series Switchmode Leaded Stacked Multilayer Ceramic Capacitor



<p>Features:</p> <ul style="list-style-type: none"> Stacked design offers the high capacitance advantage of Tantalum along with extremely low ESR. 'J', 'L' and 'N' Leaded configuration, will provide mechanical and thermal stress relief. Capacitance range from 0.047 uF to 33 uF. Voltages from 25 v to 500 v. Available in NPO, X7R dielectrics Hi-Reliability testing is available For other custom size, voltage and values contact the factory. 	<p>Applications:</p> <ul style="list-style-type: none"> Power supplies DC-DC converters Surge protection Industrial control circuits Snubber Custom applications Hi-Rel Application Filtering, Smoothing and decoupling application Audio Circuits
--	--

Summary of Specification:

***Maximum Capacitance and available voltages:**

Size Π Code	EIA Chip Size	NPO Maximum Capacitance (uF)						X7R Maximum Capacitance (uF)					
		25 V	50 V	100 V	200 V	250 V	500 V	25 V	50 V	100 V	200 V	250 V	500 V
C18	1825	0.12	0.10	0.10	0.082	0.082	0.047	5.6	4.7	3.9	1.8	1.8	0.47
C28	1825	0.22	0.22	0.22	0.15	0.15	0.10	12	10	8.2	3.6	3.6	1.0
C38	1825	0.36	0.30	0.30	0.27	0.27	0.15	15	15	12	5.6	5.6	1.5
C48	1825	0.47	0.39	0.39	0.33	0.33	0.18	22	18	15	6.8	6.8	1.8
C19	2225	0.15	0.12	0.12	0.10	0.10	0.056	8.2	6.8	3.9	2.2	2.2	0.56
C29	2225	0.30	0.22	0.22	0.22	0.22	0.12	15	12	8.2	3.9	3.9	1.2
C39	2225	0.47	0.36	0.36	0.30	0.30	0.18	27	18	12	5.6	5.6	1.8
C49	2225	0.56	0.47	0.47	0.39	0.39	0.22	33	27	18	8.2	8.2	2.2

Π Stacked configuration is available on other sizes. Please contact the factory

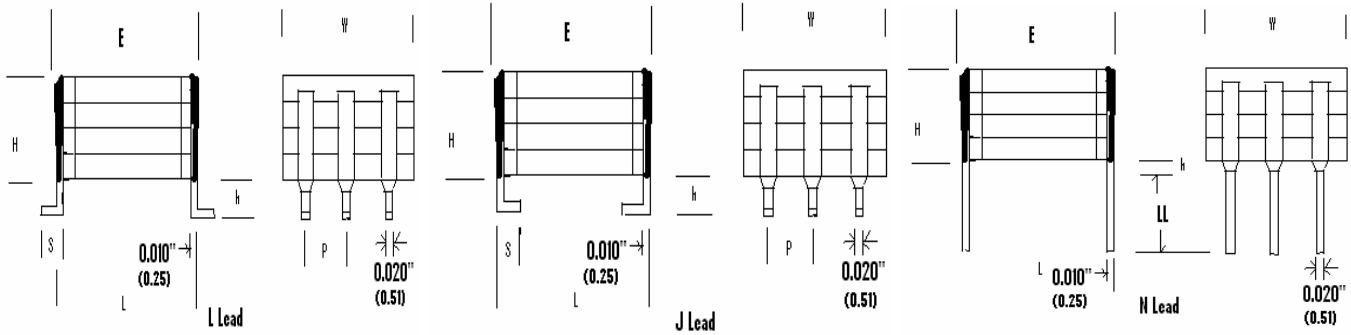
***Electrical Characteristics:**

Temperature Coefficient	X7R: $\pm 15\%$, NPO: $0 \pm 30 \text{ppm}/^\circ\text{C}$
Working Temperature	-55°C to 125°C
Insulation Resistance	100 M Ω .uF or 10G Ω whichever is less at Rated voltage
Dielectric strength voltage (DWW)	Rated Voltage (RV) $\leq 100\text{V}$: 2.5x RV 100 < Rated Voltage (RV) < 500V 2.0x RV Rated Voltage (RV) = 500V 1.5x RV
Aging	NPO: None X7R: 2.5%/Decade hr
C/DF measurement	1KHz, 1.0 vrms, 25 $^\circ\text{C}$

SC Series Switchmode Ledged Stacked Multilayer Ceramic Capacitor



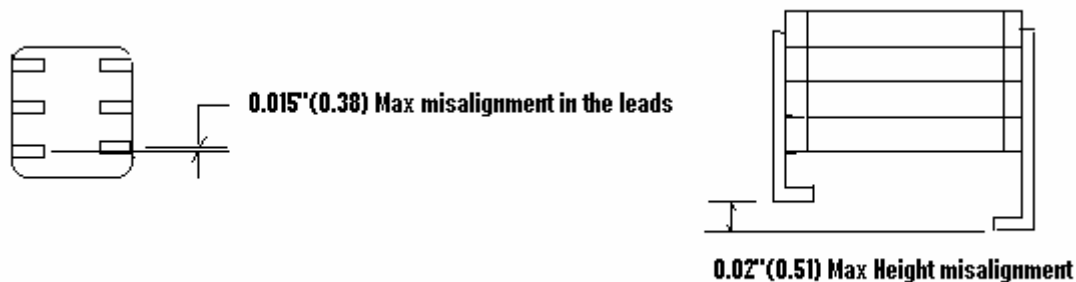
*Mechanical Characteristics:



	C18	C19	C28	C29	C38	C39	C48	C49
L±0.02(0.51)	0.21(5.33)	0.25(6.35)	0.21(5.33)	0.25(6.35)	0.21(5.33)	0.25(6.35)	0.21(5.33)	0.25(6.35)
W(Max)	0.27(6.86)	0.27(6.86)	0.27(6.86)	0.27(6.86)	0.27(6.86)	0.27(6.86)	0.27(6.86)	0.27(6.86)
H(Max)	0.10(2.54)	0.10(2.54)	0.20(5.08)	0.20(5.08)	0.30(7.62)	0.30(7.62)	0.40(10.16)	0.40(10.16)
S(typical)	0.065(1.65)	0.065(1.65)	0.065(1.65)	0.065(1.65)	0.065(1.65)	0.065(1.65)	0.065(1.65)	0.065(1.65)
P±0.01(0.25)	0.10(2.54)	0.10(2.54)	0.10(2.54)	0.10(2.54)	0.10(2.54)	0.10(2.54)	0.10(2.54)	0.10(2.54)
h*(typical)	0.070(1.78)	0.070(1.78)	0.070(1.78)	0.070(1.78)	0.070(1.78)	0.070(1.78)	0.070(1.78)	0.070(1.78)
E(Max)	0.24(6.10)	0.28(7.11)	0.24(6.10)	0.28(7.11)	0.24(6.10)	0.28(7.11)	0.24(6.10)	0.28(7.11)
LL(Min)**	0.1(2.54)	0.1(2.54)	0.1(2.54)	0.1(2.54)	0.1(2.54)	0.1(2.54)	0.1(2.54)	0.1(2.54)
# of leads per side	3	3	3	3	3	3	3	3

- All dimensions are in Inches (mm)
- The number of chips in stack varies depends on the capacitance value
- * 'h' varies depends on the lead style. See lead configuration in "How to order" section
- ** Applies only to Straight (N) leads

Other Mechanical specifications:



SC Series Switchmode Leaded Stacked Multilayer Ceramic Capacitor



*How to order:

SC	29	J	X	124	K	101	N	T
Product Code	Stack and Size Code	Lead* Configuration	Dielectrics	Rated Voltage	Tolerance	Voltage	Marking	Packaging/Special Requirement
SC: Commercial size switchmode stack	First digit: # of chips in stack Second digit: Chip size, 8=1825 9=2225	J: J lead L: L lead K: J lead (h=0.045) M: L lead (h=0.045) N: Straight lead	N: NPO X: X7R	Two significant digit + number of zero (in pF) Ex: 105: 1000000pF=1uF	F: ±1% G: ±2% J: ±5% K: ±10% M: ±20%	025: 25v 050: 50v 101: 100v 201: 200v 501: 500v	N: No Marking S: Special Marking M: Marked (Cap and Tolerance)	Blank: Standard electrical test H: Hi-Rel Testing B: Bulk T: Tape & Reel W: Waffle pack

- 1% and 2% tolerances are only available in NPO

***Soldering and Handling Precautions:**

Due to their geometry and mass, stacked ceramic capacitors have an increased susceptibility to thermal and mechanical cracks. To minimize mechanical cracks, capacitors should be handled carefully and stored in the original waffle pack container, carrier tape or other suitable container until use. Care should be taken that ceramic chips do not come in contact with each other which can cause chip outs, cracks or other mechanical damage.

The recommended method for soldering stacked chips, is reflow soldering. Wave soldering and manual soldering with an Iron is not recommended. Ceramic capacitors must be preheated and cooled at a rate less than 3°C/sec to within 50°C of the peak reflow temperature. Sudden increases, or decreases in temperature beyond the recommended rate, may cause thermal cracks.